Automatic Placement And Routing Using Cadence Encounter

Automatic Placement And Routing Using Cadence Encounter Automatic Placement and Routing Using Cadence Encounter Navigating the Labyrinth of Chip Design Imagine designing a microchip Not just any chip but a complex systemonachip SoC containing billions of transistors each needing precise placement and connections This isnt like building with LEGOs its more like navigating a labyrinthine city with millions of tiny interconnected houses each demanding its own address and delivery route for electricity and data This is where Cadence Encounter a powerful Electronic Design Automation EDA tool steps in wielding its magic wand of automatic placement and routing to bring order to this chaotic microcosm For years chip designers toiled manually painstakingly placing each transistor and meticulously drawing connections a process both incredibly timeconsuming and prone to errors It was akin to building a cathedral with a toothpick painstaking delicate and requiring years of expertise But then came the age of automation and with it tools like Cadence Encounter revolutionized the industry This article will delve into the fascinating world of automatic placement and routing within Cadence Encounter exploring its capabilities benefits and the intricacies of this crucial stage in chip design Well move beyond the dry technicalities and paint a vivid picture of how this tool tackles the complexity of modern chip design The Choreography of Transistors Understanding Automatic Placement Automatic placement in Cadence Encounter is like orchestrating a grand ballet Thousands even millions of dancers transistors and other components need to find their perfect spots on the stage the silicon wafer to minimize congestion and maximize performance The software uses sophisticated algorithms to analyze various factors the connections between components their physical dimensions and power requirements It then strategically positions each component striving for a harmonious arrangement that minimizes signal delays and power consumption Think of it as a complex jigsaw puzzle but one where the pieces are constantly shifting and the image isnt predefined Encounter uses various placement algorithms each tailored to 2 different design goals For instance one might prioritize minimizing wire length while another might focus on optimizing signal integrity

The choice of algorithm often depends on the specific chip architecture and design requirements One designer I spoke with a veteran of over two decades in the semiconductor industry recalled a particularly challenging project involving a highspeed processor Manual placement would have taken months if not years and resulted in significant signal integrity issues However utilizing Cadence Encounters advanced placement engine they completed the task within weeks achieving superior performance and reduced power consumption This anecdote perfectly illustrates the transformative power of automated placement The Road Map of Data Automatic Routings Crucial Role Once the components are placed the next challenge emerges connecting them This is where automatic routing comes into play Imagine a vast network of roads needing to be laid out to connect all the houses in our metaphorical city Cadence Encounters router acts as a sophisticated civil engineer efficiently plotting the routes for billions of signals The router faces many obstacles including obstacles like preplaced components prerouted signals and various design constraints like signal integrity requirements Encounter employs advanced algorithms to find the shortest and most optimal routes considering factors like signal delay crosstalk and power consumption Its not just about finding a path its about finding the best path balancing performance and efficiency The routers capabilities are truly remarkable It can handle complex signal routing intricate clock networks and highspeed interfaces all while adhering to strict design rules and manufacturing limitations The process is iterative with the router constantly refining its routes based on congestion and other factors Its a constant negotiation and optimization akin to air traffic control ensuring smooth and efficient flow of data Beyond the Basics Advanced Features and Capabilities Cadence Encounter boasts a wealth of advanced features that extend beyond basic placement and routing These include Congestion Management Intelligent algorithms proactively identify and mitigate potential congestion hotspots before they become critical issues Signal Integrity Analysis Encounter incorporates advanced tools to analyze and optimize signal integrity ensuring reliable signal transmission Power Optimization Features designed to minimize power consumption crucial for battery powered devices 3 Design Rule Checking DRC and Layout Versus Schematic LVS Builtin tools to ensure the layout meets design rules and accurately reflects the schematic Integration with other Cadence tools Seamless integration with other Cadence tools allowing for a streamlined design flow These advanced features enable designers to create more efficient highperformance and reliable chips They transform the process from a tedious

errorprone undertaking to a sophisticated efficient and ultimately more creative endeavour Actionable Takeaways Embrace Automation Leverage the power of automatic placement and routing tools like Cadence Encounter to dramatically reduce design time and improve efficiency Understand the Algorithms Familiarize yourself with the different algorithms and their strengths and weaknesses to choose the optimal settings for your project Iterative Design Remember that placement and routing are iterative processes Continuously monitor and refine your design to achieve optimal results Leverage Advanced Features Explore the advanced capabilities of Cadence Encounter to address specific design challenges and optimize performance Invest in Training Proper training and continuous learning are essential to fully utilize the power of Cadence Encounter Frequently Asked Questions FAQs 1 Is Cadence Encounter suitable for all types of chip designs Cadence Encounter is a versatile tool used across a broad range of chip designs from simple to highly complex SoCs However the specific configuration and algorithms might need adjustments based on the design complexity and requirements 2 How long does it take to learn Cadence Encounter The learning curve depends on prior experience with EDA tools However dedicated training and handson practice are essential for effective use 3 What are the system requirements for running Cadence Encounter Cadence Encounter requires significant computing resources including powerful processors ample RAM and substantial disk space The specific requirements depend on the complexity of the design 4 How does Cadence Encounter handle design changes during the placement and routing process Cadence Encounter offers robust capabilities to handle design changes allowing for iterative design and refinement However significant changes might necessitate rerunning portions of the placement and routing processes 4 5 What are the licensing options for Cadence Encounter Cadence Encounter is a commercial EDA tool and licensing options vary depending on usage and organizational needs Contact Cadence directly for detailed licensing information In conclusion Cadence Encounters automatic placement and routing capabilities are transformative for the semiconductor industry Its a powerful tool that enables designers to navigate the intricate complexities of modern chip design ultimately leading to more efficient highperformance and reliable chips By embracing its power and understanding its capabilities designers can unlock new levels of innovation and efficiency in their work

VLSI Placement and Routing: The PI ProjectRouting, Placement, and

PartitioningPlacement and Routing of Electronic ModulesVLSI Placement and RoutingMechanisms for Tighter Integration of Placement and RoutingIntegrated Placement and Routing for VLSI Layout Synthesis and OptimizationAn Integrated Placement and Routing ApproachIntroduction to Place and Route Design in VLSIsParallel Algorithms for Placement and Routing in VLSI DesignOptimal Placement for River RoutingPartitioning, Placement, and Routing Algorithms for High Compelexity Integrated CircuitsPlacement and Routing for Reconfigurable SystemsPerformance Driven Placement and Routing AlgorithmsNovel Algorithms for Placement and Routing and Their Parallel ImplementationsImproved Detailed Placement and Routing Methodologies and Optimizations for Advanced Technology NodesA Placement and Routing Algorithm for a New High Throughput FPGA ArchitectureNew Approaches to Standard Cell Placement and RoutingVLSI Placement and Global Routing Using Simulated AnnealingPlacement and Routing Algorithms for Hierarchical Integrated Circuit LayoutGlobal Routing and Channel Routing in P.A.R.A.D.E. (Placement and Routing Automated Design Environment). Alan T. Sherman George Winston Zobrist Michael Pecht Alan Theodore Sherman Devangkumar Jariwala University of California, Berkeley. Computer Science Division Min Pan Patrick Lee Randall Jay Brouwer Charles E. Leiserson Ren-Song Tsay Piotr Stepien Tong Gao Zhaoyun Xing Bangqi Xu Rahul Ray Peter R. Suaris Carl Sechen Stanford University. Computer Systems Laboratory Gregorio T. Jr Gervasio

VLSI Placement and Routing: The PI Project Routing, Placement, and Partitioning Placement and Routing of Electronic Modules VLSI Placement and Routing Mechanisms for Tighter Integration of Placement and Routing Integrated Placement and Routing for VLSI Layout Synthesis and Optimization An Integrated Placement and Routing Approach Introduction to Place and Route Design in VLSIs Parallel Algorithms for Placement and Routing in VLSI Design Optimal Placement for River Routing Partitioning, Placement, and Routing Algorithms for High Compelexity Integrated Circuits Placement and Routing for Reconfigurable Systems Performance Driven Placement and Routing Algorithms Novel Algorithms for Placement and Routing and Their Parallel Implementations Improved Detailed Placement and Routing Methodologies and Optimizations for Advanced Technology Nodes A Placement and Routing Algorithm for a New High Throughput FPGA Architecture New Approaches to Standard Cell Placement and Routing VLSI Placement and Global Routing Using Simulated Annealing Placement and Routing Algorithms for Hierarchical Integrated

Circuit Layout Global Routing and Channel Routing in P.A.R.A.D.E. (Placement and Routing Automated Design Environment). *Alan T. Sherman George Winston Zobrist Michael Pecht Alan Theodore Sherman Devangkumar Jariwala University of California, Berkeley. Computer Science Division Min Pan Patrick Lee Randall Jay Brouwer Charles E. Leiserson Ren-Song Tsay Piotr Stepien Tong Gao Zhaoyun Xing Bangqi Xu Rahul Ray Peter R. Suaris Carl Sechen Stanford University. Computer Systems Laboratory Gregorio T. Jr Gervasio*

this book provides a superb introduction to and overview of the mit pi system for custom vlsi placement and routing alan sher man has done an excellent job of collecting and clearly presenting material that was previously available only in various theses confer ence papers and memoranda he has provided here a balanced and comprehensive presentation of the key ideas and techniques used in pi discussing part of his own ph d work primarily on the place ment problem in the context of the overall design of pi and the contributions of the many other pi team members i began the pi project in 1981 after learning first hand how dif ficult it is to manually place modules and route interconnections in a custom vlsi chip in 1980 adi shamir leonard adleman and i designed a custom vlsi chip for performing rsa encryp tion decryption 226 i became fascinated with the combinatorial and algorithmic questions arising in placement and routing and be gan active research in these areas the pi project was started in the belief that many of the most interesting research issues would arise during an actual implementation effort and secondarily in the hope that a practically useful tool might result the belief was well founded but i had underestimated the difficulty of building a large easily used software tool for a complex domain the pi soft ware should be considered as a prototype implementation validating the design choices made

with rapid advances in vlsi technology the routing problem has come to assume a position of significance and is one of the most widely investigated problems in vlsi design automation specific elements included in the discussion are the library cell approach slicing topology and aspects of layout automation such as the placement and partition problem

this practical guide presents and compares the fundamental theories and techniques of placement and routing and provides important new approaches to solving specific

problems focusing on highly reliable methods for good manufacturing capability placement and routing of electronic modules discusses the mathematical basis for placement and routing including set combinatorial and graph theories explicates the definitions structures and relationships of tree types and gives methods of finding minimum trees furnishes useful techniques for placing and routing high density modules supplies ways to determine the work space area needed for placement and routing shows how to estimate the number of layers necessary to complete routing explains via minimization to reduce work space area facilitate manufacture and reduce the number of layers demonstrates a variety of search strategies for paths connecting two nodes on a work space with obstacles and much more containing over 300 illustrative examples figures and tables that clarify concepts and enhance understanding placement and routing of electronic modules should be a useful tool for electrical and electronics mechanical reliability process and manufacturing engineers computer scientists applied mathematicians and graduate level students in these disciplines

within this framework we propose a set of global routing optimization techniques to optimize routability we also propose a set of simultaneous placement and routing spr optimization techniques for congestion optimization the techniques are very general and can accomodate complex objective functions e g routing overflow routed wirelength maximum via density we have built optimization engines based within the trunk decomposition framework and report promising results for both the standard cell and the fpga domains

this dissertation investigates ways to integrate various vlsi layout algorithms via carefully designed integrated data structures such an integrated approach can achieve better overall results by iterating non sequentially among the various algorithms in a demand driven manner the shared data strucure which is modified incrementally by all the different algorithms serves as an efficient communication medium between them this approach has resulted in several new prototype tools including a new placement program that combines wire length optimization with a new 2 d compaction algorithm a new area routing approach that employs hierarchical rip up and reroute techniques in an integrated global and detailed routing environment and also a system that integrates the area router with a placement adjustment algorithm this integrated system can iterate automatically between area routing and placement adjustment phases to

generate optimized results for macro cell problems with over the cell routing

the book is organized in seven chapters physical design flow timing constraints place and route concepts tool vendors process constraints timing closure place and route methodology and flow eco and spare gates formal verification coupling noise chip optimization and tapeout

the computational requirements for high quality synthesis analysis and verification of vlsi designs have rapidly increased with the fast growing complexity of these designs past research has focused on the development of heuristic algorithms special purpose hardware accelerators or parallel algorithms for the numerous design tasks to decrease the time required for solution in this thesis we propose two new parallel algorithms for two vlsl synthesis tasks standard cell placement and global routing the first algorithm a parallel algorithm for global routing uses hierarchical techniques to decompose the routing problem into independent routing subproblems that are solved in parallel results are then presented which compare the routing quality to the results of other published global routers and which evaluate the speedups attained the second algorithm a parallel algorithm for cell placement and global routing hierarchically integrates a quadrisection placement algorithm a bisection placement algorithm and the previous global routing algorithm unique partitioning techniques are used to decompose the various stages of the algorithm into independent tasks which can be evaluated in parallel finally we present results which evaluate the various algorithm alternatives and compare the algorithm performance to other placement programs and we present measurements on the parallel speedups available

programs for integrated circuit layout typically have two phases placement and routing the router should produce as efficient a layout as possible but of course the quality of the routing depends heavily on the quality of the placement on the other hand the placement procedure ideally should know the quality of a routing before it routes the wires in this talk we present an optimal solution for a practical common version of this placement and routing problem author

applications using reconfigurable logic have been widely demonstrated to offer better performance over software based solutions however good performance rating is often destroyed by poor reconfiguration latency time required to reconfigure hardware to

perform the new task recent research focus on design automation techniques to address reconfiguration latency bottleneck the contribution to novelty of this thesis is in new placement and routing techniques resulting in minimising reconfiguration latency of reconfigurable systems this presents a part of design process concerned with positioning and connecting design blocks in a logic gate array the aim of the research is to optimise the placement and interconnect strategy such that dynamic changes in system functionality can be achieved with minimum delay a review of previous work in the field is given and the relevant theoretical framework developed the dynamic reconfiguration problem is analysed for various reconfigurable technologies several algorithms are developed and evaluated using a representative set of problem domains to assess their effectiveness results obtained with novel placement and routing techniques demonstrate configuration data size reduction leading to significant reconfiguration latency improvements

abstract as technology advances the effect of intra module delays become less significant while the effect of inter module interconnection delays become more prominent also as power dissipation becomes an important issue in vlsi design it is desirable for the signals to arrive at the inputs of the modules at the same time in order to reduce the number of unwanted transient switches to minimize the signal arrival times at the primary ouput pins and the signal skews at the inputs of the modules we developed a net based performance driven placement algorithm and a path based performance driven placement algorithm as chip architectures become more specific e g fpga it is important to consider the physical design information during logic design steps therefore we developed a placement driven technology mapping algorithm for fpga circuits finally as technology advances interconnection wires are placed in closer proximity and circuits operate at higher frequencies consequently reduction in crosstalks between interconnection wires becomes an important consideration in vlsi design to satisfy the crosstalk constraints and to minimize the total crosstalk among all the nets in a design we developed a track permutation algorithm for gridded channel routing problems we also developed a wire segment assignment algorithm for both channel routing problems and switchbox routing problems the experimental results indicate that our algorithms are very promising

in advanced technology nodes aggressive device scaling along with fundamental physical lithographic patterning cmp reliability variability etc and circuit crosstalk delay

etc limitations remain as a result ever more complex design rules introduce challenges for the design automation tool flow especially placement and routing p r moreover as feature sizes shrink there is increased difficulty of modeling the behavior of devices as the proximity of devices significantly affects device performance the increasing complexity and difficulty lead to three challenges first turnaround times of both automated design tool flow and manufacturing increase due to i model hardware miscorrelation and ii miscorrelation in different p r tool stages second direct application of academic works is limited because research works focus more on abstracted and simplified problems while leaving the key elements of such abstraction and simplification as open questions third the gap between academia and industry is widening because academic works tackle highly dependent problems with independent and disjoint efforts for example the open literature is dominated by isolated research works on global routing and detailed routing where the crucial correlation between these stages is ignored to address these three challenges this thesis presents research works in three directions i detailed placement optimization for correlation improvement ii key elements of enablement for routing in advanced technology nodes and iii an open source end to end global detailed routing tool that gives a first ever academic routing flow for advanced technology nodes to improve correlation with detailed placement optimization this thesis presents two works i an optimal multi row detailed placement optimization for neighbor diffusion effect mitigation and ii an in route pin access driven detailed placement refinement for detailed routing convergence improvement to enable academic research on routing this thesis presents two works on key elements i a geometry based design rule check engine and ii a dynamic programming based pin access analysis engine to narrow the gap between academia and industry in routing this thesis presents an end to end complete routing flow for advanced technology nodes implementation of the routing flow along with the aforementioned design rule check engine and pin access analysis engine are open sourced under a permissive license

from my b e e degree at the university of minnesota and right through my s m degree at m i t i had specialized in solid state devices and microelectronics i made the decision to switch to computer aided design cad in 1981 only a year or so prior to the introduction of the simulated annealing algorithm by scott kirkpatrick dan gelatt and mario vecchi of the ibm thomas 1 watson research center because prof alberto

sangiovanni vincentelli my uc berkeley advisor had been a consultant at ibm i re ceived a copy of the original ibm internal report on simulated annealing approximately the day of its release given my background in statistical mechanics and solid state physics i was immediately impressed by this new combinatorial optimization technique as prof sangiovanni vincentelli had suggested i work in the areas of placement and routing it was in these realms that i sought to explore this new algorithm my flj st implementation of simulated annealing was for an island style gate array placement problem this work is presented in the appendix of this book i was quite struck by the effect of a nonzero temperature on what otherwise appears to be a random in terchange algorithm

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